

FIG. 1

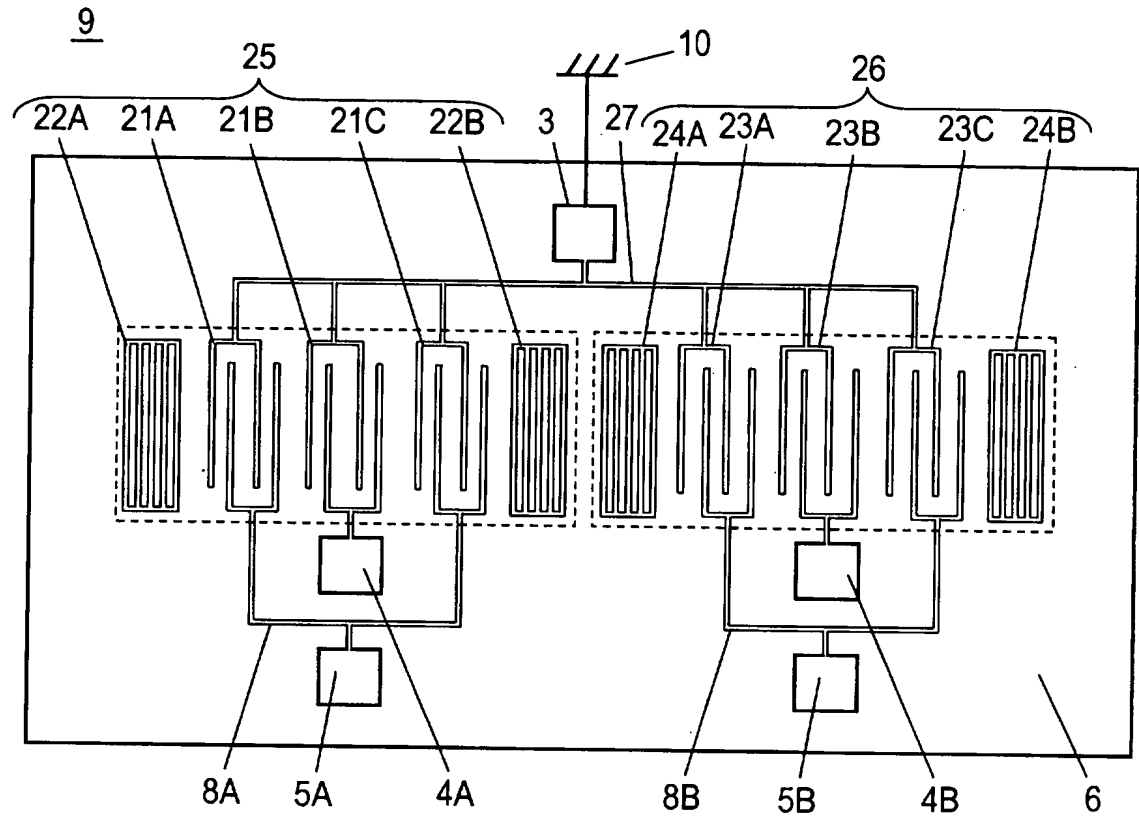


FIG. 2

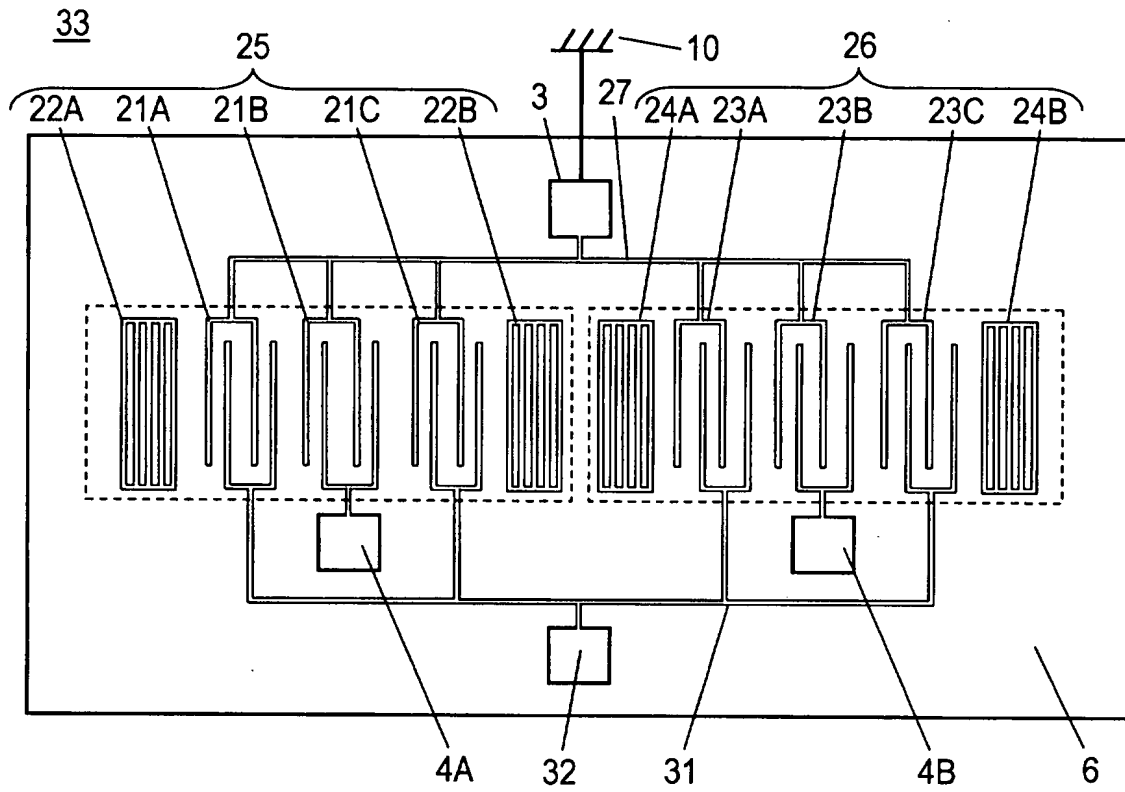


FIG. 3

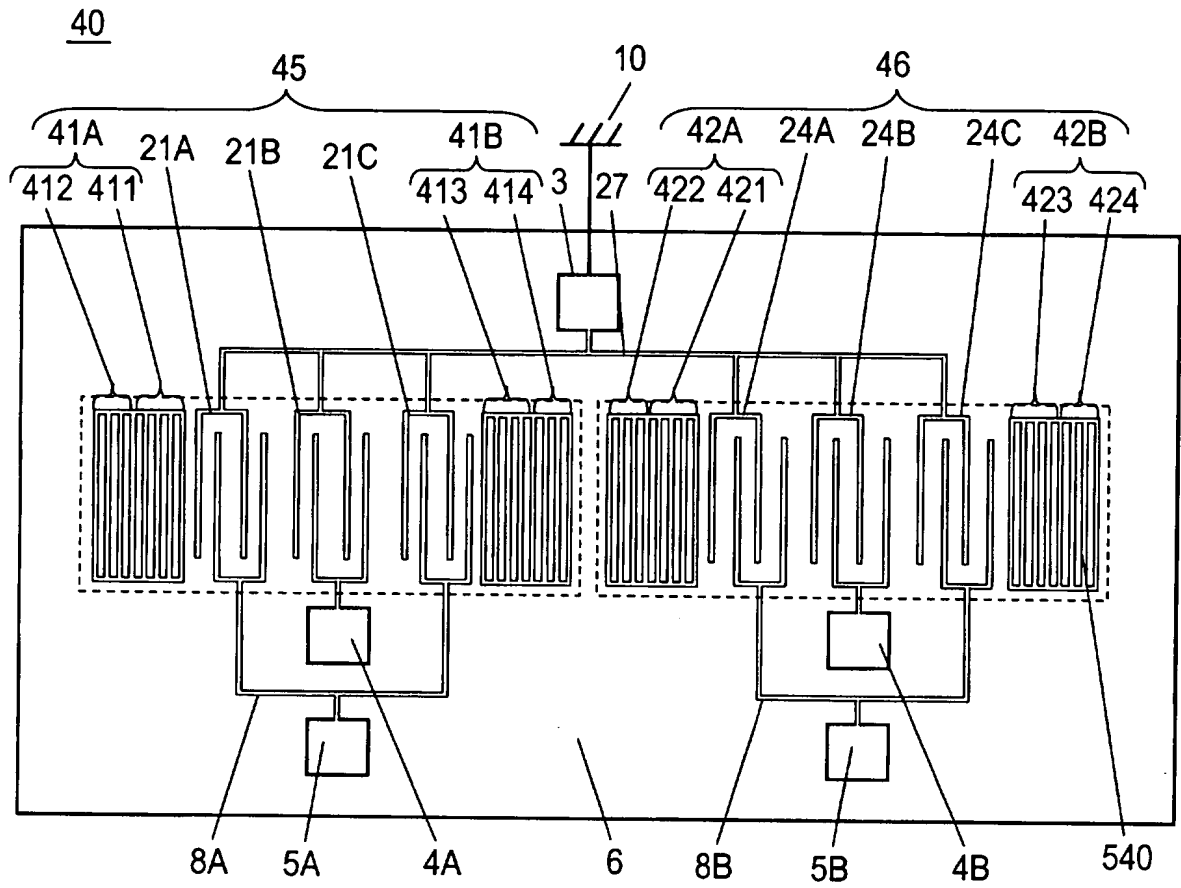


FIG. 4

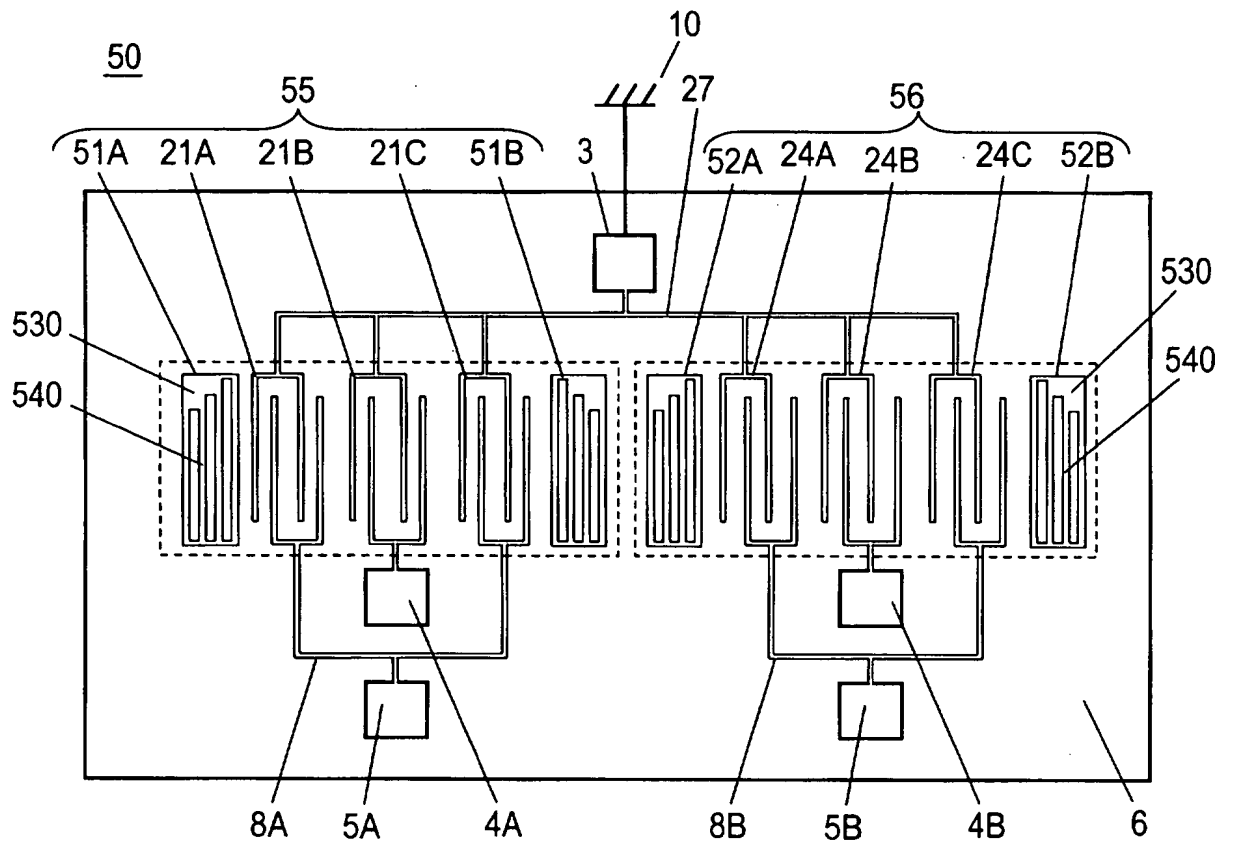


FIG. 5

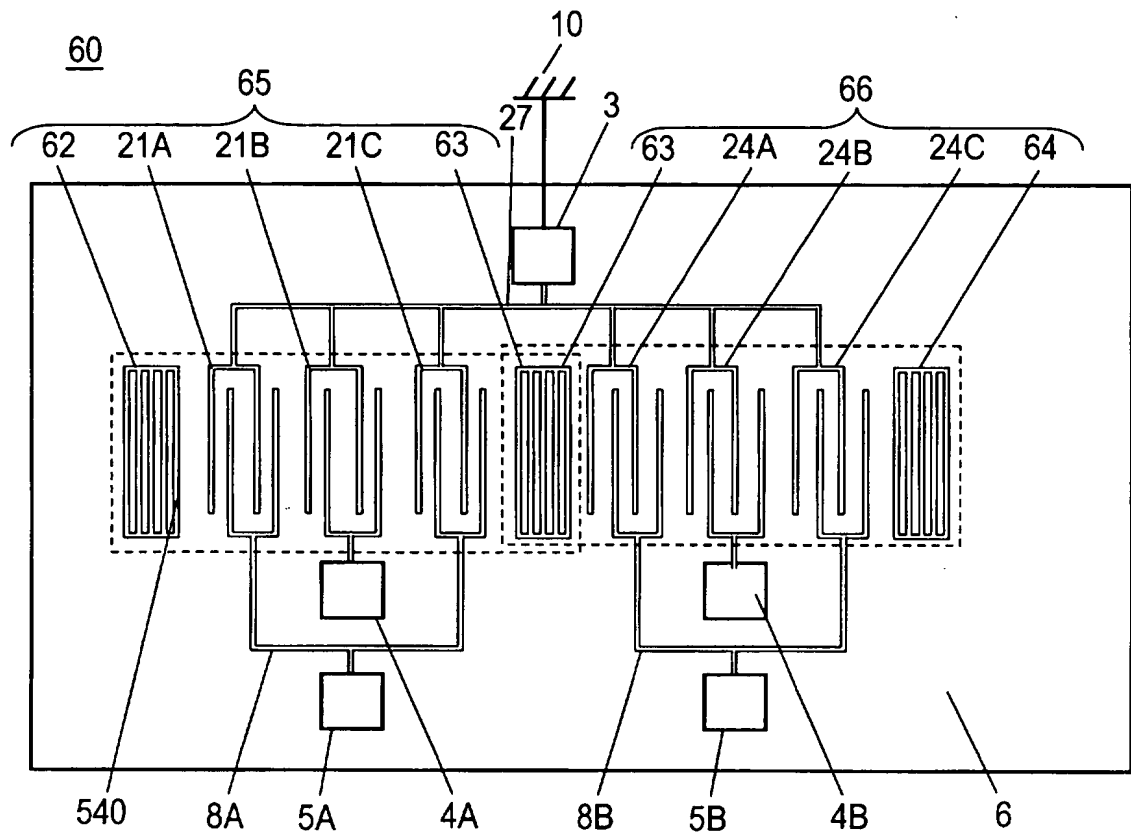


FIG. 6

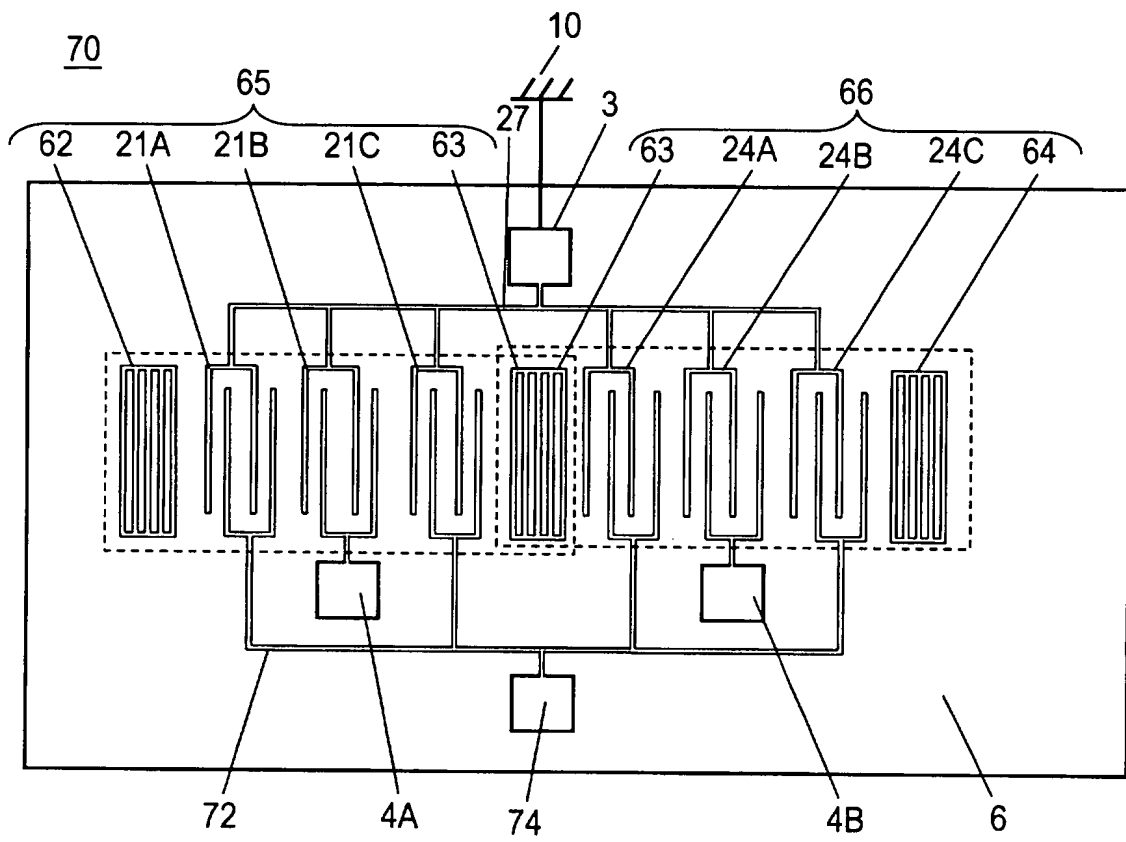


FIG. 7

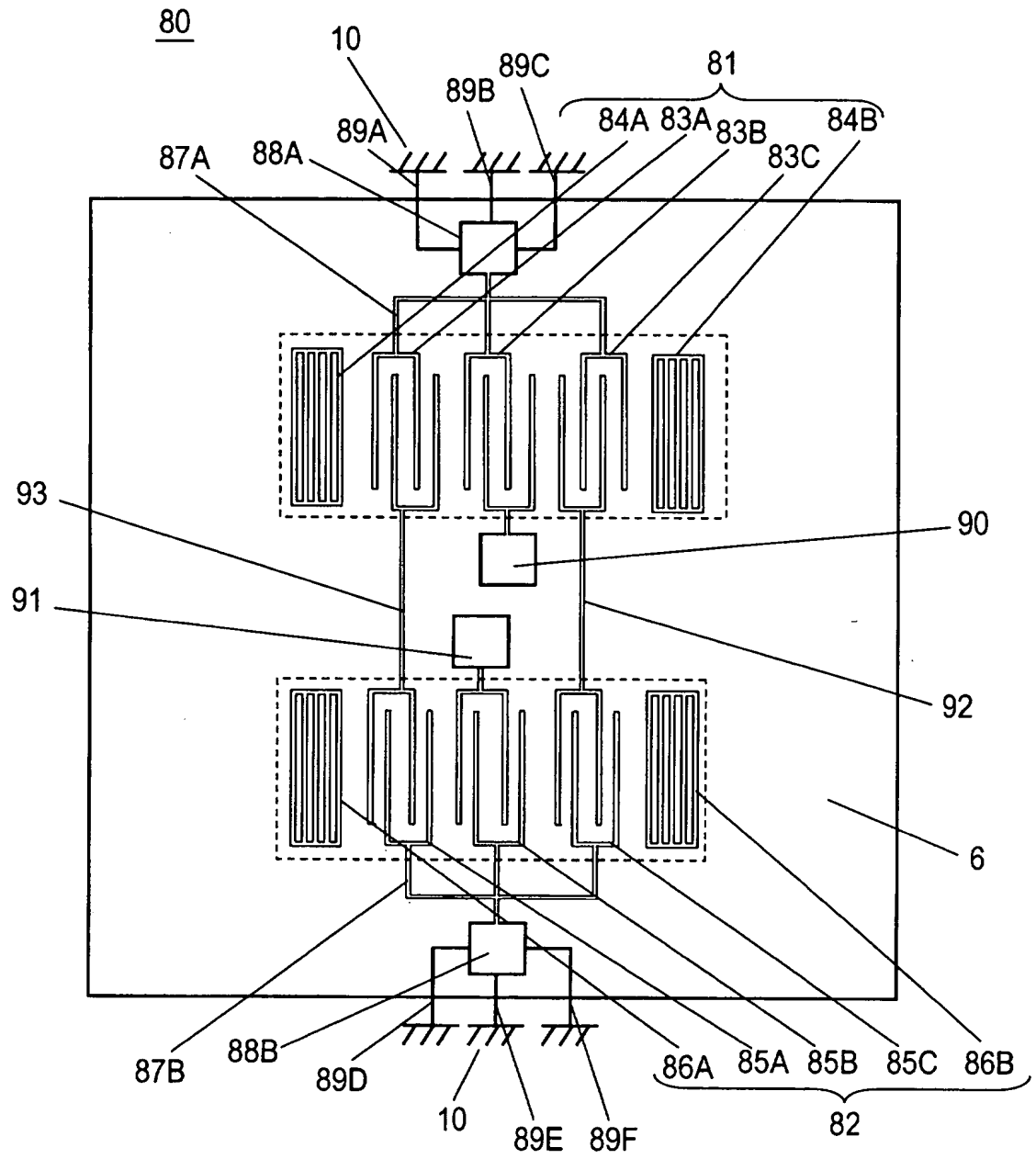


FIG. 8

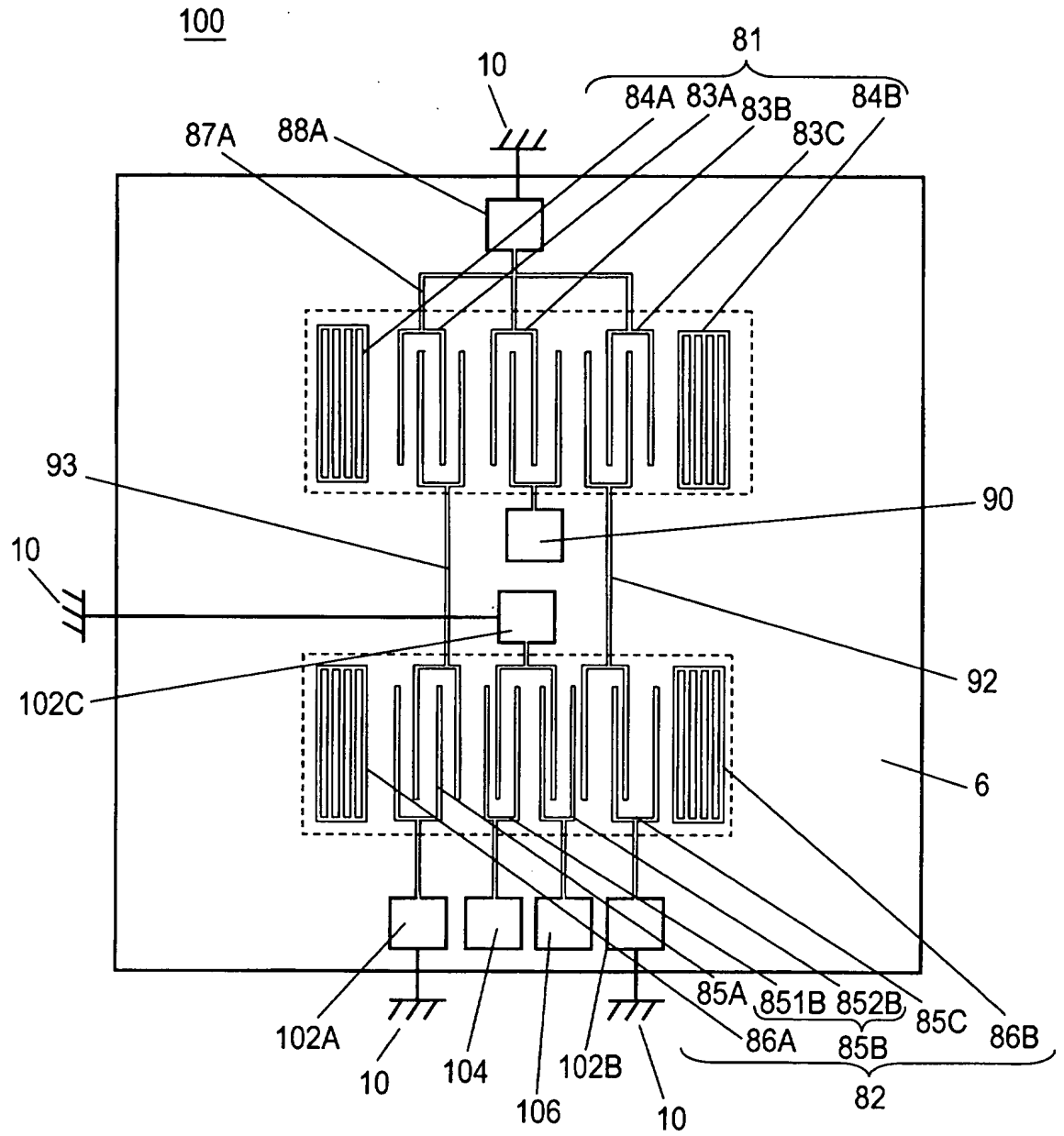
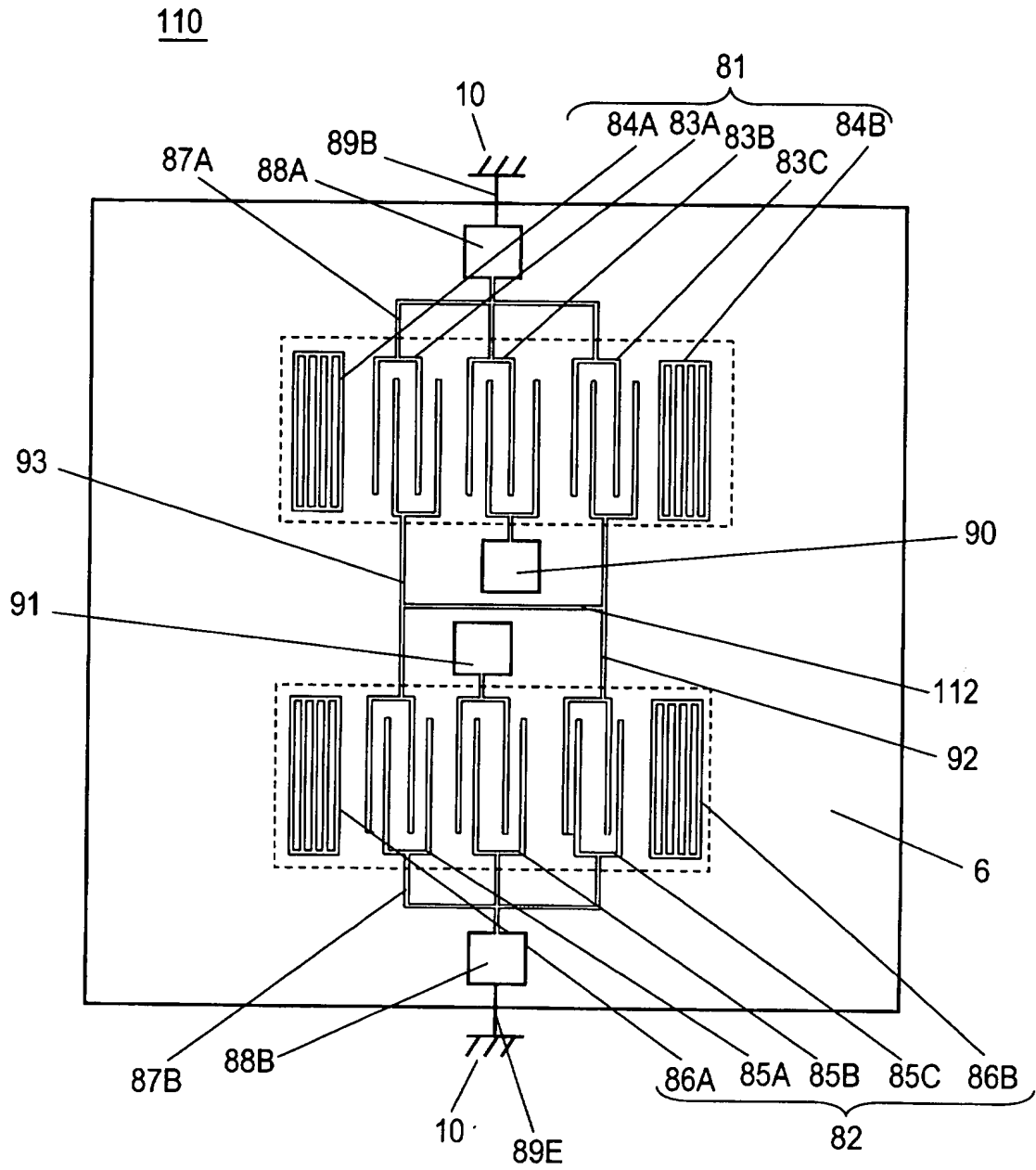




FIG. 9



The schematic diagram illustrates a semiconductor device 10, which is a 2x2 array of unit cells 6. Each unit cell 6 is a rectangular structure containing a vertical stack of layers. The layers are labeled as follows: 120 (top layer), 121 (gate layer), 122 (gate layer), 123 (channel layer), and 124 (bottom layer). The device includes various components labeled with reference numerals: 125A, 125B, 125C, 126A, 126B, 127A, 127B, 127C, 128A, 128B, 129, 130, 131A, 131B, 131C, 132A, 132B, 133A, 133B, 133C, 134A, 134B, 135, 136, 137, 138, 139, 140, 141, 142, 143, 144, and 145. The device is connected to a power supply 10 and ground 136.

FIG. 11

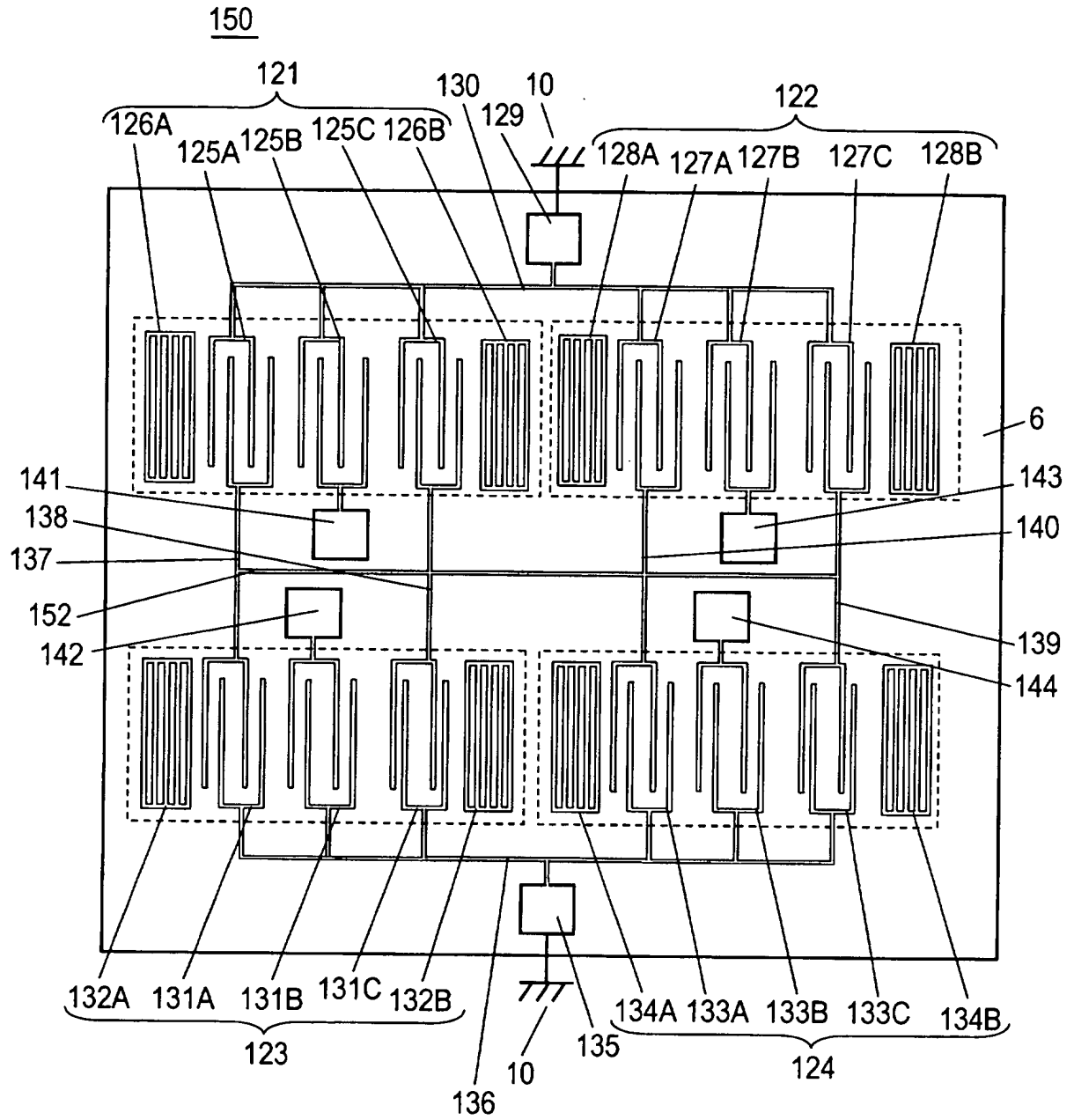


FIG. 12

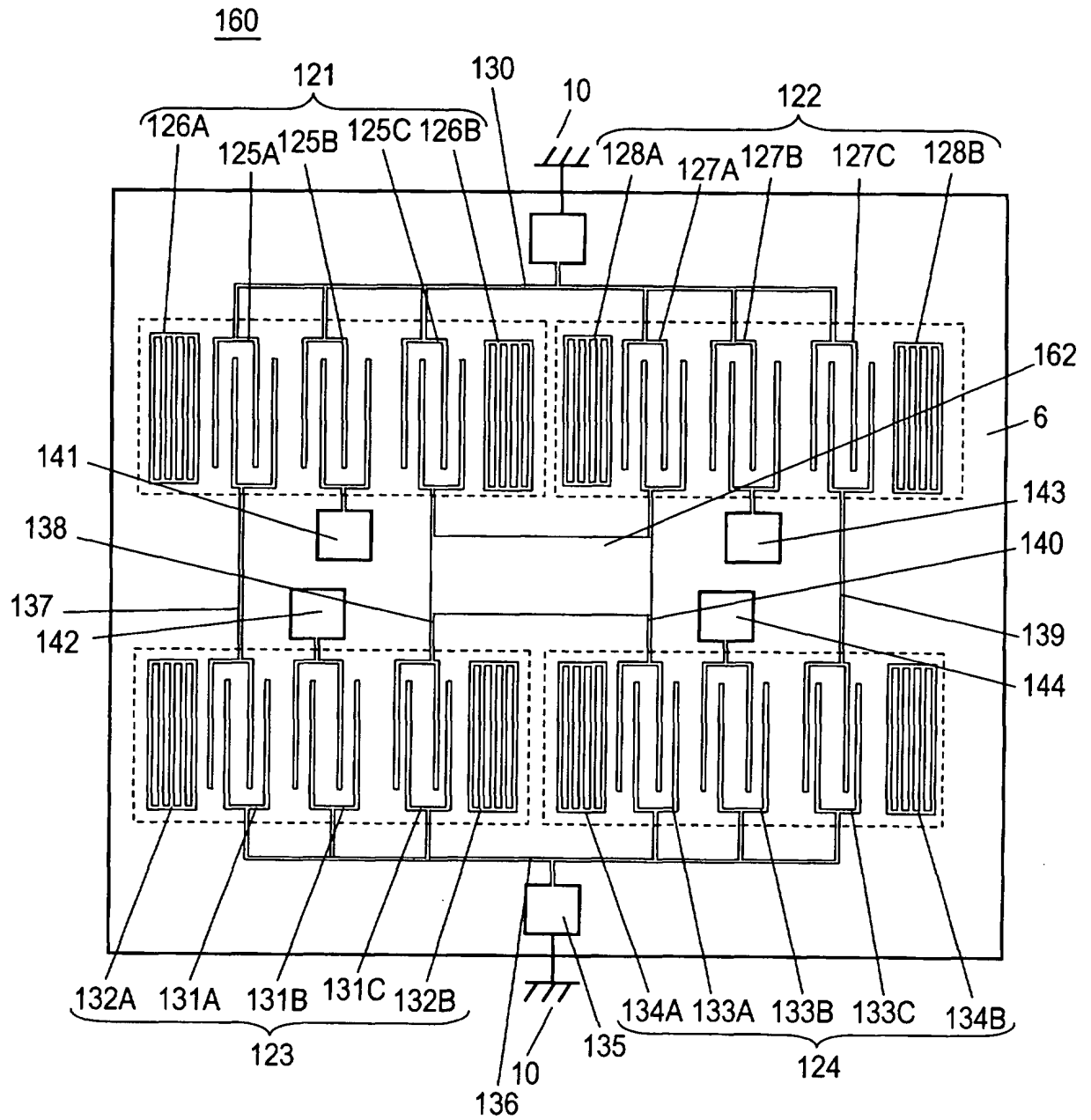


FIG. 13

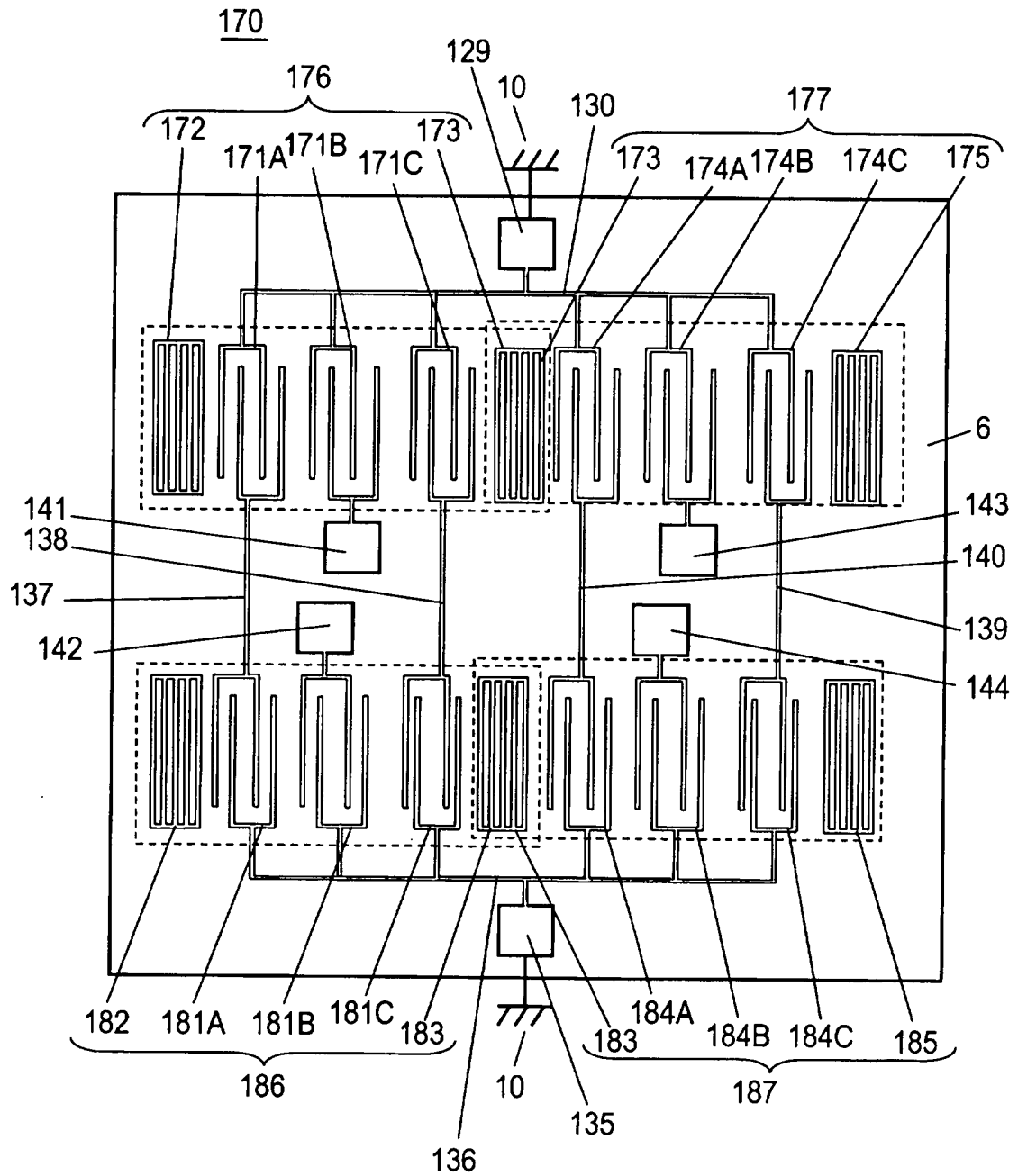


FIG. 14

